UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,637	12/14/2000	H. Peter Hofstee	AUS920000345US1	2284

7590 10/19/2004

DILLON & YUDELL LLP
8911 NORTH CAPITAL OF TEXAS HIGHWAY
SUITE 2110
AUSTIN, TX 78759

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,637	HOFSTEE, H. PETER	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004 and 06 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 and new claims 12-17 considered. Claims 1-8 have been amended as per Applicant's request. Claims 9-11 have been canceled as per Applicant's request. New claims 12-17 have been added as per Applicant's request.

Claim Objections

2. Claims 12, 13, and 17 are objected to because of the following informalities: Please write full name of signals "ack" and "req" to clarify meaning of signals to system.. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dean, U.S. Patent Number 5,544,342 (herein referred to as Dean) in view of Lefsky et al., U.S. Patent Number 4,949,249 (herein referred to as Lefsky).

5. Referring to claim 1, Dean has taught a two-phase asynchronous pipeline comprising:

a. A control path for generating asynchronous data transfer control signals according to a multiple phase protocol (Dean column 10, lines 48-49 and 51-57; column 23, lines 50-62; Figure 4; and Figure 14b); and

b. A pulse generator interface coupled between said control path and said data path and operable to translate both rising and falling edges of the data transfer control

signals into data transfer pulses (Dean column 19, lines 41-43; column 23, lines 23-37; Figure 10; and Figure 12).

6. Dean has not taught

a. A data path comprising a plurality of processing stages for sequentially processing data, the processing stages interleaved with a plurality of latching stages for holding and propagating the data between the processing stages;

b. Said control path comprising a plurality of sequentially coupled control elements.

7. Leftsky has taught

a. A data path comprising a plurality of processing stages for sequentially processing data, the processing stages interleaved with a plurality of latching stages for holding and propagating the data between the processing stages (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5);

b. Said control path comprising a plurality of sequentially coupled control elements (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5).

8. A person of ordinary skill in the art at the time the invention was made, and as taught by Leftsky, would have recognized that the latches compensate for large amounts of clock skew in a pipelined system (Leftsky column 1, lines 58-68), thereby ensuring data coherency and correctness. Therefore, a person of ordinary skill in the art at the time the invention was made

would have recognized that incorporating the latches of Leftsky in the device of Dean ensures data coherency and correctness.

9. Referring to claim 2, Dean has taught wherein said latching stages comprise level-sensitive latches for holding and propagating data through said data path (Dean column 8, lines 17-18; column 10, lines 47-6; column 15, lines 14-36; Figure 2; Figure 4; and Figure 9).

10. Referring to claim 3, Dean has taught wherein said pulse generator interface comprises dual-pulse generator means that delivers a data transfer pulse to said latching stages in response to both said rising and said falling edges of said data transfer control signals (Dean column 23, lines 23-37; Figure 10; and Figure 12).

11. Referring to claim 4, Dean has taught wherein said control element comprise Muller C-elements (Dean column 15, lines 14-36; column 21, lines 42-46; column 22, line 55 to column 23, line 5; Figure 9; and Figure 10).

12. Referring to claim 5, Dean has taught wherein said pulse generator means comprises a plurality of dual-pulse generators each comprising:

a. A logic gate having a first input and a second input, wherein said first input is connected to the output of one of said control elements (Dean column 23, lines 22-37 and Figure 12); and

b. A delay element connected between the output of said control elements and said second input, wherein a pulse is produced at the output of said logic gate in accordance with the delay imparted on said data transfer control signal by said delay element (Dean column 23, lines 22-37 and Figure 12).

13. Referring to claim 6, Dean has taught wherein said logic gate is a XOR gate (Dean column 23, lines 22-37 and Figure 12).

14. Referring to claim 7, Dean has taught wherein said delay element comprises an even number of inverters (Dean column 23, lines 50-62; column 50, lines 22-28 and 50-56; Figure 12; Figure 13; Figure 39; Figure 40; and Figure 41). In regards to Dean, the delay element is adjusted to delay the desired amount of time, so, when the system wants to delay equivalent to a gate, then four inverters will be used.

15. Referring to claim 8, Dean has taught a pipeline control circuit for providing asynchronous two-phase data transfer control, said pipeline control circuit comprising:

a. A plurality of sequentially coupled C-elements for providing sequential data transfer control among the plurality of data processing stages, wherein each of said plurality of sequentially coupled C-elements includes a control output, a first input coupled to the control output of a preceding control element, and a second input coupled to the control output of a subsequent control element(Dean column 15, lines 14-36; column 21, lines 42-46; column 22, line 55 to column 23, line 5; Figure 9; and Figure 10);

b. A plurality for dual-pulse generators each receiving as input the control output from a corresponding one of said plurality of C-elements, each of said dual-pulse generators translating signal transition from the control outputs of said C-elements into latch control pulses applied (Dean column 19, lines 41-43; column 23, lines 23-37; Figure 10; and Figure 12).

16. Dean has not taught a data path having a plurality of sequential data processing stages interleaved with a plurality of latching stages for holding and propagating data between the processing stages. Leftsky has taught a data path comprising a plurality of processing stages for sequentially processing data, the processing stages interleaved with a plurality of latching stages for holding and propagating the data between the processing stages (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5). A person of ordinary skill in the art at the time the invention was made, and as taught by Leftsky, would have recognized that the latches compensate for large amounts of clock skew in a pipelined system (Leftsky column 1, lines 58-68), thereby ensuring data coherency and correctness. Therefore, a person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the latches of Leftsky in the device of Dean ensures data coherency and correctness.

17. Referring to claims 12-14, Dean has not taught

a. Wherein each of said plurality of control elements includes a control output, a req input coupled to the control output of a preceding control element, and an ack input coupled to the control output of a subsequent control element (Applicant's claim 12);

b. Wherein at least one of said control elements is characterized as changing logic states on its control output responsive only to both req and ack inputs changing state (Applicant's claim 13); and

c. Wherein for each of said sequentially coupled control elements said control path further comprises a delay element coupled between the req input and the control output of the preceding control element (Applicant's claim 14).

18. Leftsky has taught

a. Wherein each of said plurality of control elements includes a control output, a req input coupled to the control output of a preceding control element, and an ack input coupled to the control output of a subsequent control element (Applicant's claim 12) (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5);

b. Wherein at least one of said control elements is characterized as changing logic states on its control 'output responsive only to both req and ack inputs changing state (Applicant's claim 13) (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5); and

c. Wherein for each of said sequentially coupled control elements said control path further comprises a delay element coupled between the req input and the control output of the preceding control element (Applicant's claim 14) (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5).

19. A person of ordinary skill in the art at the time the invention was made, and as taught by Leftsky, would have recognized that the latches compensate for large amounts of clock skew in a pipelined system (Leftsky column 1, lines 58-68), thereby ensuring data coherency and correctness. Therefore, a person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the latches of Leftsky in the device of Dean ensures data coherency and correctness.

20. Referring to claim 15, Dean has taught wherein each of said dual-pulse generators is coupled between a control output of one of said control elements and a corresponding latching stage (Dean column 19, lines 41-43; column 23, lines 23-37; Figure 10; and Figure 12).

21. Referring to claim 16, Dean has taught a method for implementing an asynchronous two-phase data transfer protocol between Stages in a micropipeline, said method comprising:

a. Utilizing a control path comprising sequentially coupled control elements to asynchronously generate data transfer control signals according to a multiple phase protocol (Dean column 10, lines 48-49 and 51-57; column 23, lines 50-62; Figure 4; and Figure 14b);

b. Utilizing a pulse generator interface coupled between said control path and said data path to translate both rising and falling edges of the data transfer control signals into data transfer pulses (Dean column 19, lines 41-43; column 23, lines 23-37; Figure 10; and Figure 12); and

c. Applying the data transfer pulses (Dean column 19, lines 41-43; column 23, lines 23-37; Figure 10; and Figure 12).

22. Dean has not taught sequentially processing data within a data path having a plurality of processing stages, wherein the processing stages are interleaved with a plurality of latching stages for holding and propagating the data between the processing stages. Leftsky has taught sequentially processing data within a data path having a plurality of processing stages, wherein the processing stages are interleaved with a plurality of latching stages for holding and propagating the data between the processing stages (Applicant's claim 14) (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5). A person of ordinary skill in the art at the time the invention was made, and as taught by Leftsky, would have recognized that the latches compensate for large amounts of clock skew in a pipelined system (Leftsky column 1, lines 58-68), thereby ensuring data coherency and correctness. Therefore, a person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the latches of Leftsky in the device of Dean ensures data coherency and correctness.

23. Referring to claim 17, Dean has not taught wherein said control path comprises a. plurality of sequentially coupled control elements each having a control output, a req input coupled to the control output of a preceding control element, and an ack input coupled to the control output of a Subsequent control element, and wherein at least one of said control elements is characterized as changing logic states on its control output responsive only to both req and ack inputs changing state. Leftsky has taught wherein said control path comprises a. plurality of sequentially coupled control elements each having a control output, a req input coupled to the control output of a preceding control element, and an ack input coupled to the control output of a

Subsequent control element, and wherein at least one of said control elements is characterized as changing logic states on its control output responsive only to both req and ack inputs changing state (Applicant's claim 14) (Leftsky column 1, lines 17-21 and 41-54; column 2, lines 3-41; column 2, line 63 to column 3, line 14; column 4, lines 53-62; column 7, lines 3-30; Figure 1; Figure 3; Figure 4; and Figure 5). A person of ordinary skill in the art at the time the invention was made, and as taught by Leftsky, would have recognized that the latches compensate for large amounts of clock skew in a pipelined system (Leftsky column 1, lines 58-68), thereby ensuring data coherency and correctness. Therefore, a person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the latches of Leftsky in the device of Dean ensures data coherency and correctness.

Response to Arguments

24. Examiner withdraws objection to the title in favor of the amended title

25. Examiner withdraws objections to the drawings in favor of the amended specification and drawings.

26. Applicant's arguments with respect to claims 1-8 and 12-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Sato, U.S. Patent Number 5,465,334, has taught a pipeline with latches.

b. Mills et al., U.S. Patent Number 5,592,435 and 5,684,752, has taught a sequential pipeline with latches and control logic.

c. Heikes et al., U.S. Patent Number 5,740,181, has taught a sequential pipeline with latches.

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
18 October 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100